【Speakers】

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【Q&A】

Q: Do you still maintain the outlook that the CY2024 WFE market will recover to CY2022 levels, as you mentioned in the last earnings briefing in May? What is the background for it?

A: We haven't changed our WFE outlook. I still think that the WFE market in CY2024 will be similar to CY2022 level. At this moment, the WFE market for memory, especially for NAND, is in a period of adjustment. But we expect DRAM to recover starting at the end of this year and NAND starting at the middle of next year.

I believe that the main driver of WFE market growth in CY2024 will be datacenter servers, given the increase in data traffic, new investments and the replacement cycle demand for servers. We estimate that CAGR of datacenter-related investment will be about 6% over the next five years. New servers are expected to feature new CPUs such as Intel's Sapphire Rapids. These new CPUs are 2.3 times larger than the current ones. In addition, the demand for GPUs along with CPUs in datacenters will accelerate due to generative AI. In terms of DRAM, DDR5 chips will be about 10% larger than the DDDR4 chips. We are already receiving inquiries about equipment related to generative AI.

Q: In the memory field, how much commercial opportunity do you see for the introduction of new equipment amidst technology migration; from DDR4 to DDR5 for DRAM and the number of layers increasing to more than 300 for NAND? Is there a possibility that existing equipment will be utilized, and new equipment will not be purchased than expected?

A: In the case of DRAM, customers tend to purchase the latest equipment for critical processes and use existing equipment for non-critical processes in line with technology migration. We expect the same to happen with NAND.

Q: Recently, the Dutch government came out with some new regulations regarding exports to China of advanced scanners, in lockstep with the US government. The US government also recently announced restrictions on exports to China of GPUs used in generative AI. How do you think these new regulations and export restrictions will impact TEL's business outlook?

A: The situation is changing constantly, and we are staying on top of it. In any case, we believe the impact

will be limited, as most Chinese customers have already taken the regulations into account and have changed their strategies. Now they are shifting their focus to mature nodes, and in fact, inquiries to us for mature nodes have been increasing.

Q: What will it take to create new technologies that solve the latest critical challenges, and what advantages do you have over your competitors in terms of bringing these technologies to the market?
A: Our advantage is that we have a comprehensive portfolio of products; in etch, deposition, clean, coater/developer, and prober. The process tools are used in both front end of line and back end of line, and probers are used in testing. This provides us with integrated knowledge between process steps, which by being shared with our customers, contributes in achieving the final device structure. We also utilize machine learning to optimize processes, for a definite advantage over our competitors.

Q: There is increasing attention on “More than Moore.” The diverse market is growing, and requirements are expected to further diversify. What is TEL's strategy for this area?
A: As mentioned in the keynote speech, we put forward our vision of "A company filled with dreams and vitality that contributes to technological innovation in semiconductors". We have tools for both front-end and back-end, and utilizing this knowledge, we will contribute in expanding the market together with our customers.

Q: What is TEL's strategy in packaging? Is TEL considering both wafer-to-wafer and die-to-wafer, and what is the market outlook for die-to-wafer?
A: Wafer-to-wafer bonding is used for CMOS image sensor and DRAM high bandwidth memory (HBM) . We are starting evaluations for NAND and logic; we expect the number of applications to grow. Wafer-to-wafer bonding has productivity benefits compared to die-to-wafer bonding, but it will not be suitable for all the products customers come up with, as the dies could have different sizes and/or shapes for heterogeneous integration of various functionalities.
TEL's packaging strategy is to pursue both wafer-to-wafer and die-to-wafer bonding, providing flexibility to our customers. We are working on die-to-wafer bonding utilizing our wafer-to-wafer bonding technology, preparing a new chip-carrier technology and considering module-system solutions.

Q: You showed a capital intensity (WFE investment based on 100k wafer starts per month) chart a few years ago. As the industry moves from 7nm to 5nm to 3nm, capital intensity increases. Will capital intensity continue to increase for logic, DRAM and NAND?
A: We have calculated capital intensity over time, and as customers migrates technology, each migration requires more process steps, which increased capital intensity. There was a big increase in the transition from 7nm to 5nm due to the adoption of EUV. GAA is expected to be adopted in the transition from 3nm to 2nm, but it will only add single-digit number of steps out of a total of about 1,000 steps. So, the impact

on capital intensity will be limited, and this benefits both semiconductor suppliers and SPE suppliers as it will help maintain the motivation to migrate technology. TEL will continue its efforts to minimize costs.

Q: High-NA Lithography: The introduction of high-NA lithography has been stalled. What are the challenges, and what is the timeline?
A: We expect testing and implementation of the technology to start in April 2024, and HVM beyond CY2025. High-NA lithography enables higher resolution, leading to finer pitches, but also results in a shallower depth of field, requiring thinner resist thickness. This requires additional development work in EUV scanners and resists, and optimizations in downstream processes. ASML has commented they are making good progress in the development, and we do not think the barriers are very high.

Q: High-NA Lithography: What partnerships do you have for the technology?
A: TEL has 100% market share in EUV coater/developer, so we have close partnership with all of our customers. TEL is also a part of the imec-ASML collaboration, and the high-NA coater/developer is being installed in Eindhoven, in line with ASML's equipment. We are taking advantage of this to learn more in this area and the results will be shared with close partners taking part of development programs at imec.

Q: Cryogenic Etch: What is the difference between cryogenic etching versus conventional etching, and what is the competitive status in that space?
A: The conventional high aspect-ratio contact (HARC) etch technology uses fluorocarbon-based chemistry, which tends to form polymers to protect sidewalls during the process. However, the polymers deposit more at the top of the structure, limiting the transport of etch species as the process goes on, and affecting the etch profile.
With the first and second-generation of cryogenic etch, isotropic etching is suppressed by lowering the wafer temperature, adversely affecting the etch profile. In the second-generation, the process was optimized by increasing the HF ratio in the plasma, which enabled a drastic increase in etch rate. Also, the second-generation cryogenic process enables deeper etching, permitting higher 3D NAND stacking and fewer tiers. In addition, the faster process requires less power consumption per wafer.
The process chamber will have several new features; cryogenic temperature capability, plasma-density control across the wafer, and tuning by machine learning and deep learning. Key customers have already been evaluating the tool with some promising results.

Q: Cryogenic Etch: How many customers are evaluating this technology, and how long do you expect they will need to for the evaluation?
A: Major 3D NAND customers have started evaluation, with some promising results. As for the evaluation period, customers will first take 2 or 3 years to adapt the technology. Over that time, both we and our customers will accumulate learning on productivity and reliability, and the tool will have become more

mature.

Q: Cryogenic Etch: What applications could the technology be applied to, other than 3D NAND?
A: Our highest priority is in 3D NAND channel hole application but are also exploring other applications to adapt this technology. We aim to gain share in the etch market with this new technology.

Q: Cryogenic Etch: How many layers can this technology be applied to, and when will it be adapted to HVM?
A: We expect it will be used with etch depths of more than 7-9μm, starting as early as CY2024. The number of layers, implementation timing, and strategy will vary from company to company.

Q: Cryogenic Etch: You mentioned that the etch rate is faster. Can you share your estimates of the potential increase in monthly wafer capacity, or the number of tools you will be able to eliminate with the technology?
A: This largely depends on which generation device the customers will adapt the technology, but generally speaking, if the etch rate is 2.5 times faster, it will process that many more wafers in the same fab space.

Q: Are there any other technologies TEL is focusing on, that you would like to share?
A: We have been working on a patterning solution to replace double patterning EUV. While EUV lithography is essential for scaling, the cost remains a challenge when using it with double patterning. Our solution uses the Gas Cluster Ion Beam (GCIB) technology to reshape EUV resist or hard mask patterns directly. The tool is already at customer site, with some good results.