【Speakers】

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Deputy General Manager, Corporate Innovation Division	Akihisa Sekiguchi
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Moderator: Koichi Yatsuda (VP, IR Department)

Yatsuda: Now it's time for us to start our Fireside Chat as a follow-up session to the Tokyo Electron IR Day held on October 12 last year. Thank you very much for joining us today despite your busy schedule. My name is Koichi Yatsuda of the IR Department, acting as a moderator for today's session.

Thanks to your support, the IR Day was well attended and very well received. However, due to time constraints, we were not able to answer questions from many of those who raised their hands during the Q&A session after the presentation. In order to be able to answer as many questions as possible in this Fireside Chat, as announced in the email, we have collected questions from investors and analysts in advance and organized the areas of interest. Today, the IR Day speakers will be answering the questions that have been organized. Please note that due to the large number of questions we received, we will not have time to answer additional questions live today. Thank you in advance for your understanding.

Please listen to today's Fireside Chat, and if you have any additional questions, please leave them in the questionnaire afterwards. We will follow up with you at a later date.

Thank you again for joining us today, and enjoy the session.

Speaker: Toshiki Kawai (President & CEO)
Moderator: Koichi Yatsuda (VP, IR Department)

Yatsuda: Let's begin by asking the CEO, Mr. Kawai to answer some of the questions we received in advance from investors and analysts regarding the outlook for the Wafer Fab Equipment(WFE) market as a whole and the corporate strategy. Thank you very much for your time, Mr. Kawai.

Kawai: Thank you.

Yatsuda: The first question is about the WFE market. The WFE market grew significantly last year in 2021 and is expected to continue to grow in the future. What do you think is the background to the expected stable growth compared to the past?

Kawai: In a nutshell, I think it means that society is becoming increasingly digitalized. In the 1990s, we were PC-centric, and in the 2000s, we became mobile-centric, but now we are shifting to data-centric, and I think the major difference is that we have shifted from "products" such as PCs and smartphones, to "products" plus "value" with the spread of IoT, AI, and 5G. Looking back at last year, the WFE market was expected to have grown by close to 50% year-on-year, backed by the fact that 5G is finally becoming widespread and a variety of applications are emerging. Looking to the future, we will see the spread of industrial IoT, such as autonomous driving and smart fabs, post-5G, and then 6G. With that in mind, data traffic is expected to grow at a CAGR of 26% per year from 2020 to 2030. In order to process such a huge amount of data, higher capacity, higher speed, higher reliability and lower power consumption are required, which means that the demand for semiconductors will continue to grow and technological innovation will be required. The semiconductor chip market, which reached 500 billion US dollars last year, is expected to double to 1 trillion US dollars by 2030, but considering that the WFE market will grow along with the semiconductor chip market, we believe that the market will continue to grow stably from a macro perspective. To make a long story short, I think the key phrase is the progress of digitalization, which has changed from "products" to "products" plus "value".

Yatsuda: Thank you for your answer. The next question is coming from another question related to the one you just answered. In addition to the applications you mentioned in your answer to the previous question, the metaverse has recently become a topic of discussion as a driver of demand. Please let us know if TEL is working on any special project teams, business development, or corporate branding.

Kawai: I mentioned earlier that a variety of applications are emerging with IoT, AI, and 5G, and the metaverse is one of these new applications. So, I have high expectations for it in terms of stimulating demand for semiconductors. As for the next question about whether there are any special activities targeting the metaverse, we do not have any. However, Tokyo Electron is also planning to make great use of digital transformation. We believe that digital transformation will also help us improve our various services, such as improving the performance of our equipment. There have been many restrictions, including travel since the spread of the new coronavirus infection. On the other hand, Tokyo Electron has 76 bases in 18 countries, and this digital transformation and remote support using VR/AR has led to quicker service and improved service efficiency. The semiconductor chip market will continue to grow, and even if the 76 bases in 18 countries I mentioned earlier become 100 bases in 18 countries, I believe that this kind of remote support will be extremely useful in providing quick support. Tokyo Electron is promoting activities to use digital transformation to improve equipment performance and service.

Yatsuda: Thank you. I would like to ask one more question related to the WFE market. The capital markets are always concerned about downside risk. What if the growth scenario of the WFE market were to collapse? What non-macroeconomic factors could be expected to play a role?

Kawai: I believe that the most important thing in forecasting market trends in the midst of great change is to capture the mega-trends. I think that the global trend toward the future will be the powerful implementation of ICT and digital transformation to build a strong and resilient society where economic

activities do not stop under any circumstances. At the same time, I believe that the trend toward decarbonization and global environmental protection, or in short, the trend toward the future, is to make digital and green compatible. In order to make digital and green compatible, it is the technological innovation of semiconductors that is very important, and we believe that the technological innovation of semiconductors will not stop. Under this circumstance, the most important thing is to have the ability to lead the world in technological innovation. And as is the case with Tokyo Electron, it is important to have a strong financial base and continue to invest in R&D, and not be short-sighted.

Yatsuda: The next question is about production and procurement. Some say that Tokyo Electron has been able to manage procurement relatively well amid the global supply chain disruption. What are your policies and plans for increasing production capacity in the future?

Kawai: Market growth, and then, at TEL itself, the delivery of new products to customers has been proceeding smoothly. As a result, we plan net sales of 1.9 trillion yen for the current fiscal year. Along with such expansion in the scale of our business, the amount of procurement has also increased significantly. We believe that our approach to procurement is becoming more important than in the past. TEL holds semi-annual production trend briefings at each plant to explain the current year's plans and production plans to its partners. In addition, the entire group holds a “Partners’ Day” once a year during the timing of SEMICON Japan at the end of the year to explain the production plan for the following year. I believe that this approach has led to proactive preparation, resulting in winning a good evaluation. As the WFE market continues to grow, we need to keep a close eye on the fact that there is a shortage of parts and components, and I think it is extremely important to utilize the production trend briefing sessions that we have built up so far in an improved manner. In addition, in light of the recent situation, we established the Corporate Production Division in September last year. By addressing this issue at the corporate level, we would like to reflect the investment plans of our customers for the next two to three years, which are understood by the sales division, in our procurement as well, so that we can achieve overall efficiency and level out the entire supply chain under more proactive procurement. With regard to this procurement, we launched an initiative called E-COMPASS last year in order to tackle environmental conservation throughout the supply chain, rather than simply securing parts and components. We have established the Corporate Production Division in order to implement environmental initiatives along with our procurement plan. Through these efforts, we hope to continue to realize proactive procurement in the future.
As for the second question about production expansion, I think the simple answer is that we will continue to invest. Last year, new production facilities went into operation in Yamanashi and Tohoku, increasing production by 1.5 times and 2 times respectively. In light of our customers' future investment plans and fab construction plans, in a nutshell, we are in a situation where we need to continuously acquire land and construct new buildings at all of our domestic plants. And we are now considering our capital investment plans.

Yatsuda: Thank you for your answer. Next, we received a question from a slightly different angle, and I would like to hear your answer. The question is, "What is the charm of Tokyo Electron?" I believe this is a question to the effect of why investors should own shares of TEL instead of other companies in the same industry. Could you please tell us about the attractiveness of TEL as a public company to invest in from the perspective of the capital market?

Kawai: As I mentioned earlier, I explained the importance of technological innovation in semiconductors for processing huge amounts of data, but the patterning process is essential to improve the performance of semiconductors. We are the only company in the world that has all four key patterning processes, and we also have a wide range of equipment for packaging and testing modules. In terms of the number of installed base equipment, we have shipped approximately 78,000 units, the largest number in the world. So, it is no exaggeration to say that there is hardly a semiconductor in the world that does not pass through TEL's equipment. I am proud of the fact that TEL is unique in this respect. And while I've talked about the importance of the leading-edge technology of semiconductors today, if you think about semiconductor devices around the world, 70% of the wafer area is manufactured with so-called legacy

tools that are not leading edge. As I mentioned earlier, we have the largest installed base record in the world, and for this area, we need new equipment, but field support and field solutions are very important. In this area, TEL has incorporated a business model in which the installed base equipment becomes a new business opportunity and generates value. I think this is rather an attractive point of TEL from the perspective of the capital market. Also, from an ESG perspective, we have received high evaluations from leading ESG evaluation organizations around the world, and I believe that one of our attractions is that our shares are included in leading ESG constituent stocks.

Yatsuda: The next question is about human resources. In the semiconductor industry, the shortage of human resources is becoming even more pronounced. What is TEL's approach to dealing with such tight labor market conditions? In addition, we have also received questions about salary design to maintain employment competitiveness, such as, "How does the salary level for general employees and engineers compare to global competitors?" Could you please answer these questions?

Kawai: As I have already mentioned, the trend toward the future is to make digital and green compatible, and in this context, technological innovation in semiconductors is becoming increasingly important. TEL will leverage its expertise as a manufacturer of semiconductor production equipment to promote and pursue technological innovation in semiconductors, thereby contributing to the world's shared value of being both digital and green. At the same time, we are striving for medium- to long-term profits and continuous enhancement of corporate value through our activities. I believe that it is very important to secure human resources by firmly demonstrating medium- to long-term profits and continuous improvement of corporate value. Through such activities, we hope to be the leader in technological innovation in all industries and the development of a prosperous society with dreams, as well as to achieve globally accepted corporate governance and ROE. With such high growth potential, we are committed to being a company with dreams and vitality. In this sense, motivation-oriented management is critical. In order to be motivated, employees need to have high expectations for the future of their company, a strong financial base, the opportunity to take on challenges without fear of failure, competitive compensation when results are achieved, fair personnel practices, and openness. These are important. As a person involved in management, I am strongly aware of this. As I mentioned about globally competitive compensation, we have adopted performance-linked compensation. And thanks to our recent high performance, we have been in the first or second place in terms of bonus level among the companies listed on the first section of the Tokyo Stock Exchange for the past few years. I am proud to say that the compensation of our general employees is at a high level from the perspective of global competitiveness.

Yatsuda: Thank you very much for your answer. This is the last question. It is a question related to governance. Why doesn't TEL have a CFO position?

Kawai: The CFO position is one option. I am not denying it, but this industry is characterized by rapid technological innovation. Under such circumstances, the continuous creation of strong next generation products with high added value is becoming extremely important. Against this backdrop of the semiconductor production equipment market, we have adopted a general manager system with multiple general managers who each have their own expertise. While monitoring market trends, we respond in an agile manner through regular review meetings such as business execution meetings and progress review meetings for medium-term plans. This is the current operating rhythm of TEL. We are seeing the progress we expect to make relative to our mid-term plan. At this time, we think it is a good idea to proceed with this method of operating. One option is to set up a CFO, CTO, or other CXO-like position, but at the moment I think the current method of operating is optimal. Also, in this industry with high growth potential, I am careful not to expose the company to the limits of growth based on the limits of my own abilities, so I am very conscious of the need to incorporate all kinds of wisdom. I have conversations with general employees through employee meetings, and I also communicate with the executive officers, so that we can always come up with the best solution for our method of operating. This type of operation is the best for us at the moment, I believe.

Yatsuda: Very well understood. Thank you very much for your time today, Mr. Kawai.

Kawai: Thank you very much.

Speaker: Sumie Segawa (Vice Division GM, Corporate Innovation Division)
Moderator: Koichi Yatsuda (VP, IR Department)

Yatsuda: Next, we will have the GM of the Corporate Innovation Division, Ms.Segawa, answer some questions regarding E-COMPASS, a supply chain initiative for the environment. Thank you very much, Ms. Segawa, for your time today. Six months have passed since TEL announced E-COMPASS last year. Can you tell us about the progress, your actual activities, and points of differentiation? Also, what are the benefits for participating companies?

Segawa: In September of last year, we established the Corporate Production Division, and have built an internal system that can be optimized across the entire group, which includes ensuring flexibility among plants for environment, procurement, quality, standard design, and element development. In addition, we shared the direction of specific activities with our partner companies at our “Partners’ Day” in December. We have held individual briefings for several partner companies with whom we have particularly close relationships, and they have viewed our activities favorably and agreed to work with us on common KPIs. Since the circumstances of each partner company vary, we will continue to provide detailed explanations and responses to gain their support for our activities. As for the open call for technologies that contribute to improving environmental performance, some companies have already applied, so I think we are off to a good start. One of our unique points of differentiation in reducing environmental impact is that we are able to share with our partners latest information on market trends and environmental laws and regulations collected globally by our company, which accounts for 85% of overseas sales. Truly valid information can be a great advantage for your business. In addition, I believe that we will be able to build a win-win relationship with our suppliers, as their products will be adopted and installed in our equipment product line, which is overwhelmingly differentiated and has a high market share. We are also planning to develop information and development infrastructures so that we can collaborate interactively with our suppliers in real time to ensure that there is no discrepancy in information. We plan to launch a dedicated website for supplier companies in the next fiscal year.
By jointly developing products that are highly competitive and compliant with laws and regulations, we expect to help improve our market competitiveness as a supplier that can provide products that customers can use with peace of mind for a long time. In addition, we would like to share not only information but also analysis methods that can be shared widely so that we can reduce the development burden on our suppliers.
Through these efforts, we will strive to provide full benefits to all participating partner companies.

Yatsuda: Thank you. I'd like to ask you a little more about the development of technologies and equipment to reduce environmental impact. Specifically, what kind of requests do you receive from customers, and what kind of technologies do you develop?

Segawa: There is a demand for equipment technology that lowers the use of resources such as energy and water, which are related to the productivity of our customers. From the perspective of productivity, this has been an issue for a long time, but in recent years, the year and specifications to be achieved have been presented more concretely, and this is becoming a competitive advantage when selecting equipment. This is due to the fact that customers themselves are becoming increasingly interested in reducing their own environmental impact, for example by sharing their vision with customers in the industrial structure, and that environmental regulations are directly related to business risks.
Proactive measures to comply with environmental laws and regulations are being proposed, and both customers and suppliers, including TEL, are accelerating their efforts to promote technological innovation. Specifically, we expect to see strong interest in film deposition equipment with energy-saving features such as improved insulation of heaters, and cleaning equipment with environmentally friendly designs that reduce and reuse the amount of water and chemicals used. We have already achieved an energy saving rate of about 30% with our energy-saving technology for piping heaters and have installed them in mass production equipment.

Yatsuda: Thank you for sharing your case study. You just mentioned that the energy efficiency of

equipment will be one of the competitive advantages in the future. Do you have any indicators to measure this? What are TEL's unique goals for the future, and what is the process for achieving them?

Segawa: As for the future activities of TEL, we plan to set milestones for 2030 and 2050 in order to realize our medium- and long-term goals.
Our medium-term environmental goal for our products is to reduce CO_2 emissions per wafer by 30% by 2030, and we have already started to improve productivity and monitor electricity, chemicals, and gases for each piece of equipment. In order to achieve the industry's top-class goal, we are determined to develop equipment with the awareness of correctly grasping the trends of environmental laws and regulations and linking them to the value of our customers in a timely manner.
In the area of environmental technology development, we have been internally implementing our own the seven key environmental issues since 2019, and we plan to collaborate with our suppliers to set goals and share the year of achievement for each item. In order to achieve the medium-term environmental goals that have already been presented, we set common KPIs with our suppliers at the recent “Partners’ Day” and confirmed that we will work on them. We plan to share a roadmap with some of our suppliers, not only on the seven key environmental issues, but also on how to develop into an environmentally advanced company together with a view to the future.

Yatsuda: Very well understood. Thank you very much for your time today, Ms.Segawa.

Segawa: Thank you.

Speaker: Akihisa Sekiguchi (Deputy GM, Corporate Innovation Division)
Moderator: Koichi Yatsuda (VP, IR Department)

Yatsuda: Next, we have some questions about TEL's technology strategy and the semiconductor manufacturing process as a whole, which will be answered by Dr. Sekiguchi, GM of the Corporate Innovation Division.

Sekiguchi: It's my pleasure to be here.

Yatsuda: Hello Aki. Since your Japanese is not as good as your English, I'd like to conduct this fireside chat in English. Are you OK with that?

Sekiguchi: Sure. You didn't have to be so straightforward, but yes. English is fine. I also understood that you went to the United States with grad school so your English would be just right.

Yatsuda: Thank you very much. OK, let's get started. First, we have received some questions regarding alliances. We have told the capital market that TEL is not only increasing its business portfolio through M&A and corporate venture capital but is also increasing business opportunities through alliances. So, first of all, what is TEL's basic approach toward alliances?

Sekiguchi: Sure. First, let me tell you why we do alliances. Right? It all has to do with the fact that today the technology is so complex that it's very difficult to actually produce the next generation and next generation technology while you try to keep in mind that you don't want too much of complexity in the process. You still need very high yields. But, at the same time you need to control the cost so much. So, if you put all those things in mind and if you think about the fact that none of the SPE makers today actually have the entire portfolio of tools. We're fortunate. Tokyo Electron, we do have a very good portfolio, but even us, we don't have all the necessary tools. And, you know what? We can do unit process well. That's for sure, but customers are increasingly demanding that we deliver more of a modular, what's called module integration approach. So, in order to do that, we have to rely on alliances and cooperation with other entities.

Yatsuda: I see. So then, what business opportunities has TEL increased through alliances so far, and what technologies do you expect in the future?

Sekiguchi: Well, let's see. For us, for Tokyo Electron, I think patterning is one of our foretastes. It's one of our strong points. If you think lithography, you require multiplicity of materials. And, you know what? You have to combine the litho process with dry etching and with wet etching or removal materials. You also have to do it with dep materials that are typically used for hard mask. So, you need to integrate all these things. If you think about how these things are combined as part of making the ICs or the circuitry design, you even have to think about things like design-technology co-optimization where you actually sort of try to get the synergies or optimize not just the design and but also with the process, right? And, if you go one step further, you also have to worry about something called DTCO versus STCO which is system-technology co-optimization. And that actually takes a whole thing from the architecture down all the way down to the process, if you will. So, those are the kind of things that we need to work on. But we're an equipment company, fundamentally. That's where our core competence is, and we have to rely on alliances know-how to deliver some of these things. So, we do have a wide range of alliances. I think the ones that you know about have to do with the announcement press release we made back in 2021 in June, I believe. It was between imec-ASML and Tokyo Electron. And it was an alliance on High-NA EUV. High-NA EUV is very critical for the future generation of logic and also DRAM for now. But, in order for us to be able to use these things, we have to rely on know-how from, of course, imec in Belgium and also the principal lithography supplier, which is ASML, the other ones who have been developing the EUV High-NA system. In other places or other alliances that come to mind or places are like IBM, Albany Nanotech. That's one of our also stronger alliances that we do talk about and have been developing, for example, the next generation gate-all-around technology as well as, it's you know, the future successor,

CFET, and so forth. And also, backside PDN, the power delivery network, this is called, is one of those things where the unit process alone won't be able to do it. It requires that we work together within the confines of consortia or with people who have better knowledge of this material. So, we do that in addition to high performance logic. We also do it for artificial intelligence type development as well as, hopefully in the future, something that includes quantum computing.

Yatsuda: OK, thanks. Let me move on the next questions I received from investors, which are related to the process integration. TEL has reported that in addition to improving the performance of individual equipment in critical processes, it is also focusing on proposing solutions through co-optimization and developing new integration schemes by exploiting a wide range of equipment lineup. So, Aki, would you tell us about some of the cases where TEL has won PORs through co-optimization of processes, and the module processes that you are currently focusing on in particular, please?

Sekiguchi: OK, let me think. I think we had a case where… this was undisclosed company, of course, but a customer we had been working on developing the latest contact module. At the time I think we had the production POR for etch process, and a sort of early production phase went on at our customer. They ran into a yield ramp up issue, and they asked us to, you know, look into the matter as well because we were the POR etch tool process supplier. And we basically discovered that when you're doing it you have to put a protective layer, you know, to control its profile. And, in doing so, this protective layer turned out to be a little difficult to remove. So, what we did was process optimization where we modified our recipes and conditions. But, at the same time we also came up with a wet process optimization. And we proposed that package together to our customer. And, lo and behold when we did an assessment on how it performed the combination of our etch and also our protective layer removal process actually worked better. So, in spite the fact that was already in a production phase we were able to turn it around, and we eventually won the POR for both in production. So, it's very difficult. It doesn't happen that often, but it does happen. And this is an example where synergy between one product that we have in another actually really worked well. But what we do try to do is to actually engage our customers very early on, and by doing so, you know, we can avoid all these problems. And, hopefully, older PORs will be ours. But we won't get that greedy, I guess. Anyway, the other things have to do more with, let's say patterning, I would say. Patterning in general, if you think about it, I think I may have mentioned it earlier, but patterning is one of those areas where you have to have both lithography know-how, etch know-how deposition know-how, and wets know-how in order to complete and deliver a package. It's like a patterning module as we used to call it that we need to deliver. And doing so, I think the fact that we do have a whole battery or combination of tools that work very well together is definitely one of those advantages and where we can take advantage.

Yatsuda: Got it. I also received a follow-up question. Let me read it. As semiconductor fabrication processes become more complex and SPE manufacturers become more oligopolistic, will the advantages and disadvantages of integrated SPE manufacturers such as TEL against specialized SPE manufacturers become more pronounced in the future? Would you please answer this question?

Sekiguchi: This is a hard question to answer. I think we all know about a company that is very good being a one product company you can be very successful if you have a very distinguished know-how or expertise in one particular area. That has been proven. Also, you also saw so, as in the previous example that there are cases when you are at an advantage when you have multiple processes and that you are at a disadvantage is because you cannot synergize with other processes. That does happen. So, it's a little hard to say definitively that this is the rule. But I think in the end it all is a matter of whether you can take advantage of what I would call treasure. TEL has a treasure called a big lineup of tools and we're fortunate in that our corporate culture is such that we work very well together, right? We have very good transparency of information between the various units. So, in patterning, lithography, etching, wets, deposition, these different BUs work very well together. And that's why we can actually take advantage of our corporate culture and mindsets in cases like this. So, this is actually two of our advantages that we do have a whole range of tools. Sometimes, if you concentrate on one thing too much, it can be a disadvantage. But if you work smartly, then it's definitely competitive advantage.

Yatsuda: Got it. Thank you, Aki. Now, we move on to the next topic. Currently, various technologies are being developed that will lead to breakthroughs in VLSI, such as High-NA EUV, 3D DRAM, and advanced packaging, which will become important in promoting scaling. I will ask about the unit process to each BU general manager, but I would like to ask you about the whole process. So, how do you think the adoption of High-NA EUV will affect Capital Intensity?

Sekiguchi: OK. Those are very long questions so I'm going to forget some of those things. So, you're going to have to remind me later on. If you think about this question, you would realize, for example, High-NA EUV, right? We asked the same question when EUV was coming on board. Is this going to affect the TAM? How is it going to disrupt the flow? But, if you look at the industry today, we're booming. All the companies are actually doing well. So, my inclination is to say that the effect on capital intensity based on High-NA EUV wouldn't be that high. I believe our CTSPS BUGM, Akiyama talked during the October IR day that even if it is introduced it's supposed to be for the N 1.5 nanometer node around 2026 for logic and logic foundry. If you recall the example back in the days EUV came, but fairly quickly. It's also the needs of having to do multi-patterning using EUV. So, although the first iteration, of course, for 1.4 or I guess people call it A14 these days. That's also going to happen in that initially it'll start by doing single exposure. But it'll quickly require something like SADP type processes. So, I don't expect the impact to be that high again from my point of view. What else can I tell you about? Let's see… The process, one of the things is tradeoff I think you can do single exposure EUV and also single exposure High-NA. There are cases where yields can be affected by whether you're using, let's say, EUV versus something like multi-patterning. So, people will start to selectively use these things. But I think that still the projection right now is that when it does get adopted High-NA EUV it should maybe be about 20% of the whole so-called EUV category with the rest 80% being the standard what you call the standard.

Yatsuda: Got it. And then, would you please tell us about the new process requirements for 3D DRAM and TEL's business opportunities?

Sekiguchi: OK. For 3D DRAM, the integration scheme or how you actually build it has not been set yet. So, we're sort of going by some of the more fairly well-known process flow. So, my discussion is based on that. So, take that with a grain of salt. From a structure point of view, you're taking something that used to go vertical, and then you're sort of putting it down. And the way people are thinking of doing that is to do sort of layers of silicon and silicon germanium epitaxially grown layered built that whole thing up. And then, what you do is you kind of come down and grow up and etch to do separation so that you can actually build individual device units, right? So that's actually going to be what we'll be doing in 3D DRAM. I think the areas that will be the focus definitely deposition, as I said, and etch, of course. But, because these are going to be very high tall structures, it might be prone, I'm guessing right now, but it might be prone to pattern collapse type of issue. And, of course, you know about our tool set that deals with high aspect ratio pattern collapse type needs. So, those are probably the processes that we will be focusing on, and also, which represents a good market for us to engage in. I think it'll be an exciting area together so well. What else have I list?

Yatsuda: You talked about DRAM. How about logic and foundries? Would you please tell us about the new technologies and business opportunities that are expected to be adopted by logic/foundries in the next five years, such as gate all-around structure and also advanced packaging?

Sekiguchi: Sure. So, let's see. Gate all-around, there are various renditions of that, right? That is also coincidentally silicon and silicon germanium epitaxial layer grown up and then sort of patterned first vertically. And then, you have to do an unisotropic very high selectivity etch in order to create the extra channel separations so forth. These are very complicated processes. It would require in addition to not just those etches that I just talked about but also ALD because it's a very complicated 3D structure. Selective processes and like I just said kind of ALD, kind of things that you would actually need to employ. However, there's a big difference between the thickness of the DRAM stack versus the gate all-around stack. Part of the reason is that for gate all-around these layers are only at the very device forming level.

They also tend to be very thin. So, from a market perspective, I think the business opportunities for Tokyo Electron are much higher when you have these other opportunities in DRAM. In fact, I think for gate all-round type devices there are discussions about doing backside power distribution network, for example. And that is likely to require, for example, our bonders because what people do is you flip the device over, and then, you sort of build up on top of the backside that wasn't used before. Part of the reason why you do that is because you want to decouple the lines that actually feed the power into the device versus the signal when you have everything coming from the top together. They tend to kind of get crowded and there's no more real estate. And also, if you look back at the history of high-performance processors, at least on logic, the trend is actually to increase the number of metallization layers. So, people, that's actually even better opportunity for us, will build up on top and we also build up on the bottom. And you know we're very strong in the backend of the line etching and so forth. So those are the kind of things that you can look.

Yatsuda: Got it. I'd like to ask you about the downside risk because investors always concern about the downsizes. So, what if the introduction of these new technologies is delayed? In the past, the EUV introduction was delayed in the past, right? Can you talk about what might be possible reasons for that?

Sekiguchi: Yeah, quite honestly, the introduction schedule these for the High-NA EUV is very aggressive by additional all parties involved. And we need this for 2026 high volume manufacturing. At least that's the current plan. So, what we do we announced this is back in 2021, right? Or actually, we started to work earlier than that, but the formal announcement came 2021. So, we've already been working on getting the elements delivered for this technology. And like I said at the very beginning alliance, "why do you do alliance?" It's because you want to reduce the risk. You also want to speed up. It's time to delivery of any kind of technology that's key. So, we call it shift left and many others also call it shift left. But what we're trying to do is accelerate the time schedule by delivering these things earlier rather than later and actually do it right. So, concept to remember time to market, shift left, collaboration, alliances, it's I make it sound like it's a great thing. It is. It is. It has its difficulties because you have many many parties to coordinate things with, but these are the kind of things that you need to do. Now, having said all the positive sides, there is a negative side. In fact, these High-NA EUV sources require even more power than before. I'm sure ASML has it under control but the other thing is it's a new type of resist that you actually need to work with High-NA EUV expose systems. In addition to that, when you go High-NA, the depth of focus also gets much much smaller. So, there are technical hurdles. And not only that. Once you've imaged it, you have to actually transfer it and then etch. And you're talking about delivering even smaller dimensions. So, in general, all these things can be very challenging and daunting when you look at the process stability, yield type issues and so forth. So, some of the things that do come to mind, but, you know, if we stay on top, I'm hopeful that things will get worked out.

Yatsuda: Thank you very much for your time today and many investors loved your presentation

Sekiguchi: So, even in English?

Yatsuda: We are looking forward to your next presentation sometime very soon, and thank you very much.

Sekiguchi: Thank you, and you're very welcome. Thank you very much.

Speaker: Keiichi Akiyama (GM, CTSPS BU)
Moderator: Koichi Yatsuda (VP, IR Department)

Yatsuda: Next, we will have the GM of the CTSPS BU, Mr. Akiyama, answer the questions regarding Coater/developer and Cleaning. Thank you very much, Mr. Akiyama. We have received many questions about the background behind TEL's ability to maintain a high level of competitiveness and a nearly 90% share of the coater/developer market. What are the factors that have enabled TEL's coater/developers to maintain such a high market share over the years, and what are your views on the sustainability of this?

Akiyama: The basis of patterning is lithography, and lithography equipment mainly consists of a coater/developer and an exposure system. The lithography process consists of coating photoresist with a coater, exposing the pattern with an exposure system, and then developing it with a developer.

Most coater/developers in mass-production fab are used in connection with exposure systems, and exposure systems are the most expensive of all process equipment. The latest EUV lithography systems cost more than 10 billion Japanese yen, so coater/developers must be highly reliable to maximize the productivity of them. The thickness of the photoresist to be coated and the line width to be developed must be controlled uniformly within and between wafers, since variations of a few nm have a significant impact on yield in the most advanced node. In particular, regarding chemically amplified photoresists, which are currently the mainstream, temperature, humidity, and the concentration of the developing solution on the wafer have a significant effect on the critical dimension (CD) of the pattern, so precise control in a coater/developer is important for pattern performance.

TEL's coater/developers have earned the trust of customers by accumulating strong past achievements in terms of both reliability and performance, and have been able to maintain the competitiveness over the years due to the collaboration with consortia and partners, and a robust system that integrates sales, marketing, field support, and plants. Semiconductors are an industry of rapid technological innovation. We maintain our competitiveness not only by making overwhelming technological differentiation with high reliability and performance, but also by quickly identifying customer needs, commercializing them, and providing them in a timely manner.

In particular, we have a 100% share of the market for coater/developers for EUV in mass production, and we plan to introduce coater/developers for high-NA EUV and metal oxide resists, which are expected to be adopted in mass production in the future.

Yatsuda: Thank you very much for explaining the factors that have allowed us to maintain a high market share in the coater/developer market. Now, I would like to move on to the question about cleaning. TEL has been able to significantly increase its share of the cleaning system market over the past several years. Please tell us about the factors that have contributed to this, including the areas in which TEL has gained market share. Also, please tell us about the technologies and areas that you are focusing on in order to achieve your target of 30% market share in the future.

Akiyama: In cleaning, we have made good progress with our business strategy in all categories and have been able to increase our market share over the past few years. In CY2020, it saw a temporary drop in TEL's share of cleaning due to customer mix, but we expect that CY2021 will surpass CY2019 level.
As we talked about our business strategy in cleaning at the medium-term management plan in May 2019, there are three main categories: single wafer cleaning, batch cleaning, and scrubbers.

First, in single wafer cleaning, there are three key technologies: bevel wet etching, preventing pattern collapse, and metal etching. Bevel wet etching has maintained a high market share since the beginning, and the market growth rate has been high, contributing to the increase in market share year by year. Regarding pattern collapse prevention technology, last year we released CELLESTA™ SCD equipped with supercritical drying technology. And, in addition to wet etching for capacitor mold removal and STI

for DRAM, we have recently received inquiries for GAA for logic. For metal etching, CELLESTA™ Pro SPM, released in 2019, is contributing to the increase in market share.

Next, in batch cleaning, we have won PORs from several companies for the critical process of wet etching of silicon nitride films and tungsten for 3D NAND, and sales are increasing.
Finally, scrubbers are becoming more important with the introduction of EUV, and we are seeing strong demand for them.

We have a relatively high share of the memory market, but there is still ample room for us to increase our share of the logic market. Our basic strategy in cleaning is not to target a wide range of generations, but to focus on the most advanced critical processes and to increase our market share by competing on the basis of technological differentiation. Fortunately, in logic, demand for bevel wet etching, where we have a high market share, and inquiries for our supercritical drying technology are becoming stronger, and by taking advantage of these opportunities, we hope to increase our market share in logic and achieve the medium-term management plan target of 30% or more.

Yatsuda: I now have a better understanding of the background and business strategy behind the increase in market share of cleaning systems. Thank you very much, Mr. Akiyama, for your time today.

Akiyama: Thank you.

Speaker: Isamu Wakui (GM, ES BU)
Moderator: Koichi Yatsuda (VP, IR Department)

Yatsuda: Next, we will have the GM of the Etch Systems Business Unit (ESBU), Mr. Wakui, answer the questions regarding etch. Thank you very much, Mr. Wakui. First, I would like to ask a question about the progress of the etch system business in relation to the medium-term management plan. According to Gartner, TEL's share of the etch system market has been on an upward trend since 2016. Looking back over the past five years, can you tell us about the factors behind the increase in market share, your progress toward the market share target in the medium-term management plan, and your strategy for the future?

Wakui: First of all, I can say that TEL's overall strategy is to focus on areas where we can leverage our strengths so that we can simultaneously increase our market share and profits. Based on this basic strategy, there are three major factors that have contributed to the increase in our share of the etch equipment market.
The first is the so-called HARC process, which etches the deep holes and trenches that are important for memory. In DRAM, we have had a high market share in the etching process for forming capacitors and high aspect ratio contacts for some time, but we have not had a high market share in the NAND channel process or the slit process for device separation. Both are HARC processes, but the materials to be etched in the channels and slits of NAND are different from the capacitors and contacts of DRAM. In 2016, when the transition from Planar NAND to 3D NAND began, we were late in developing equipment and processes. However, since then, with the cooperation of our customers, we have applied the HARC etching technology we have developed for DRAM. By introducing new technologies, we have gradually created technological superiority and improved our market share.
The second is to gain market share in the etching process for DRAM interconnects. In the past, aluminum was used as the wiring material for DRAM, but with the progress in miniaturization, copper, which has lower resistance, is now being used. Since aluminum can be dry etched, wiring is formed by directly etching aluminum. However, since copper is a material that is difficult to dry etch, holes and trenches are formed by etching the dielectric film, and copper fills these holes and trenches. This is a scheme called Damascene. This damascene scheme has been used in logic devices since the 90nm generation, and we boast an overwhelming etch share of the damascene market. With the adoption of Damascene in DRAM, we were able to apply the technology we had developed in logic and successfully gain etch market share.
The third is patterning. With the advancement of miniaturization, it has become necessary to form patterns with a density greater than that which can be defined by lithography. Fine, dense, regularly aligned lines and spaces can double or even quadruple the density of lithographically defined patterns through deposition and etch, while patterning becomes more complex. In order to improve productivity, we have developed a technology to etch dissimilar materials in a single etch step in a fine manner. Since this technology was adopted by our customers for mass production, our etch market share in the patterning process has increased. Our etch equipment market share target in the medium-term management plan is to achieve 30-35% by the fiscal year ending March 2024, and we are making good progress.
In the future, we aim to further increase our etch equipment market share and profit margin by providing even more added value. Last year, we released Episode UL.
In addition to increasing productivity per unit area, the number of chambers that can be installed per system can be selected from 4 to 12 chambers to flexibly accommodate the layout of the customer's fab. We also strive to achieve autonomous process control and would like to contribute to increase our customers' profitability by equipping an automatic parts replacement function, numerous sensors, and a high-speed control system in the etch equipment. This is achieved through big data analysis that exploits TEL's proprietary smart tools that utilize DX.

Yatsuda: Thank you for the detailed explanation about the factors behind the increase in market share and the future differentiation strategy by providing added value. Next, I would like to ask you about mature nodes, which have recently become a major factor in the semiconductor shortage. In 2021, increasing inquiries from the mature generation helped boost WFE market growth. TEL has also released a 300 mm

etch system for power devices, and the product line can cover a wide range of nodes. Would you please tell us about the background of the increasing investment in mature nodes and the competitiveness of etch systems and initiatives for mature nodes?

Wakui: Regarding memory, most of the investment is for the most advanced node, as the most advanced manufacturing technology offers the lowest cost per bit, but in logic/foundry, where there is demand for a wide range of technology nodes, inquiries for mature nodes are becoming very strong. We assume that logic/foundry will account for about 60% of the WFE market in 2021, of which about 40% will have been invested in mature nodes. The reason for the rapid growth in investment in mature nodes is that in addition to semiconductors with relatively large elements, such as power semiconductors and discrete devices for automotive and industrial applications, there has been a rapid increase in demand for semiconductors that are relatively close to the leading-edge node of 20-45nm and have high versatility, driven by AI and IoT. Automotive/industrial and general-purpose semiconductors are categorized in the same mature node, but have different technology requirements.
Our basic strategy in the etch business has been to differentiate ourselves by introducing competitive new technologies in the critical processes of the most advanced node, where technological innovation is rapid, and to gain a high market share in mature nodes by delivering used equipment and modifications. Although sales for modifications have continued to maintain a high level, the increasing demand for power semiconductors for automotive and industrial applications has depleted used equipment, resulting in a decline in sales. Therefore, we have released new equipment for these large element semiconductors. On the other hand, for general-purpose semiconductors of the 20-45nm generation, which are close to the leading edge, we sell equipment with the necessary optimal generation technology. Although the etch systems we offer are different for power semiconductors and general-purpose semiconductors, which belong to mature nodes, our approach is the same: to provide solutions by utilizing technology assets that we have developed and matured in the past. In this way, we have built a high level of competitiveness in a wide range of nodes by providing the most suitable etch systems for the types and nodes of semiconductors manufactured by our customers.

Yatsuda: Very well understood. Lastly, please tell us about the business opportunities for cutting-edge nodes. It has been some time since the limits of miniaturization have been discussed for semiconductors, but with the adoption of new structures and materials and the evolution of technology, the limits will be broken and Moore's Law will likely continue. Recently, next generation technologies such as GAA, nanosheet, CFET, 3D DRAM, Backside PDN, etc. are being talked about. What are the opportunities for TEL in etch for these new structures and materials?

Wakui: First of all, GAA and nanosheet or CFET are basically the same thing when you look at the transistor alone. Nanosheet is named after the channel structure, which is made up of layers of thin film sheets, and the structure is a GAA transistor with the entire channel covered by the gate. CFETs are made of GAA transistors stacked vertically. The main difference in etch between FinFET and GAA is whether the channel material to be etched is silicon only or layers of silicon and silicon germanium. In the case of GAA, isotropic etching of silicon germanium with a high selectivity to silicon is required, while they are quite similar to each other from a material point of view. GAA has different technology requirements than FinFET. Normally, if customers require just an extension of the technology from the conventional technology, they tend to select equipment based on past achievements. But, if customers require totally new technology, they usually select equipment based on actual performance rather than past achievements. The technology shift of GAA provides an opportunity for us to increase our market share in conductor etch equipment, where our share in conductor etch equipment is low compared to that of dielectric etch equipment. GAA is also expected to increase the demand for highly selective dielectric etching at the atomic layer level for ultra-fine contacts. Next is 3D DRAM, which, like GAA, requires bulk anisotropic etching of silicon and silicon germanium stacked films and highly selective isotropic etching of silicon germanium against silicon. However, unlike GAA, each layer of the film is thicker and has a much higher aspect ratio, making etch for 3D DRAMs a new technological requirement.
Finally, regarding backside PDNs, integration is becoming more and more important nowadays.
We aim to maximize business opportunities for TEL as a whole by developing integrations and proposing

solutions that enable backside PDN in cooperation with other equipment business units.

Yatsuda: Got it. Thank you very much, Mr. Wakui, for your time today.

Wakui: Thank you.

Speaker: Jack Ishida (GM, TFFBU)
Moderator: Koichi Yatsuda (VP, IR Department)

Yatsuda: Next, we have received questions about film formation, and I would like to ask Mr. Ishida, GM of the Thin Film Formation Business Unit (TFF BU), to answer them. Mr. Ishida, thank you very much for your time. First, I have a question about ALD, which is a fast-growing area in the deposition market. First of all, could you tell us about the characteristics of ALD?

Ishida: The basic principle of ALD is that a portion of the material which you want to deposit is adsorbed onto the surface where you want it to be deposited by a single atomic layer using self-limiting adsorption properties. Depending on the material of the substrate and the combination of raw materials to be adsorbed, pretreatment may be required. After the adsorption step, the excess material is exhausted and then reacted with another raw material, resulting in the deposition of one atomic layer of material. Only one atomic layer of material can be deposited in one cycle, and the thickness of the material to be deposited is determined by the number of cycles in the process. In general, ALD is characterized by its ability to deposit films with fine and uniform thickness even on the surface of complex 3D structures, making it an extremely suitable deposition method for miniaturization, which is the main reason for the high market growth rate. On the other hand, the time required to obtain a single atomic layer is relatively long compared to other methods such as CVD, and this results in higher costs, which is a disadvantage.

Yatsuda: I see. ALD is an ultra-thin film deposition technology that is suitable for precise film thickness control, isn't it? Tokyo Electron provides both batch and semi-batch ALDs, but we have been asked about the difference between them and single wafer ALDs. Could you please explain the difference?

Ishida: Single-wafer ALD is increasingly being adopted for mass production, with the advantage of high controllability being a priority when the respective steps of adsorption, pumping, and reaction can be shortened. However, the film thickness that can be obtained for the time required for one cycle is fixed, and the number of wafers that can be processed simultaneously is limited, resulting in relatively low productivity. On the other hand, batch ALD can process multiple wafers at the same time when more time is needed for each step to improve film quality, etc., resulting in relatively higher productivity. TEL provides two types of equipment: semi-batch ALD in addition to batch ALD. In semi-batch ALD, the wafer is passed through different processing areas rather than changing the process gas. The main difference is that different process operations are performed at the same time depending on the position of the wafer. One rotation will process one cycle. Depending on the material to be deposited, the ideal reaction time will vary depending on the combination of adsorbing and reacting materials. In batch processing, this difference is optimized by the processing time. The advantages of semi-batch are that the space size can be changed in advance for each material to be deposited, optimized in the hardware, and further optimized according to the rotation speed. One more advantage is that it expands the range of application of plasma, which is limited in batch. Batch/semi-batch ALD is widely used for memory applications due to its higher productivity compared to single-wafer ALD, but it is also being used to improve productivity in cutting-edge logic applications where capital intensity is increasing.

Yatsuda: Got it. One more question about ALD: Could you tell me the difference between ASFD, that you introduced at the IR Day in January, and single-wafer ALD?

Ishida: Instead of single-wafer ALD, we offer our proprietary technology, single-wafer ASFD. ASFD features CVD with excellent step coverage, which can deposit an ultra-thin film of several atomic layers when looking at just one cycle, but by repeating this process at high speed, ASFD is as good as single-wafer ALD in terms of step coverage performance and achieves higher productivity. Single-wafer ASFD has been widely used in the deposition of barrier metal for contacts and titanium nitride for DRAM capacitor electrodes, and has had a high market share for many years. As we introduced at the IR Day last January, we hope to take advantage of this feature in high-k dielectric films to gain market share in the future.

Yatsuda: Lastly, we have received questions about business opportunities for TEL's film deposition equipment in new devices. Would please you tell us about TEL's business opportunities and the potential for adoption by customers in changing device structures such as GAA and 3D DRAM?

Ishida: For both GAA and 3D DRAM, there is a need for layered stacking of silicon and silicon germanium, and we are trying to achieve cost breakthroughs with batch equipment. In GAA, customers are also considering adopting several ultra-thin dielectric films, which were also introduced at the IR Day, and we believe that this will be a good opportunity for us. In addition, we believe that there are new business opportunities in the adoption of backside interconnects, such as low-resistance metal deposition, etch stop films, and the modification of interlayer insulating film. For ultra-thin dielectric film, the ALD I mentioned earlier is the most promising, and we will provide the optimal film formation equipment that balances cost and performance from among batch, semi-batch, and single-wafer deposition. In improving the performance of devices with these structural changes, new performance requirements must be realized in addition to the realization of microfabrication. Therefore, we are actively developing and evaluating combinations of pre-treatment processes, such as cleaning, and post-treatment processes such as modification, with a focus on film deposition. In the process development, we are able to utilize not only our knowledge of batch and single-wafer deposition, but also the seed technologies that we have cultivated in other products such as cleaning and etching, which is a major advantage for us. In the commercialization of equipment, we will select the optimal technology of mass-production equipment from among batch, semi-batch, and single-wafer systems in terms of both cost and performance, and we will strengthen our contribution to the expansion of the semiconductor industry, which is expected to expand in all aspects.

Yatsuda: Understood. Thank you very much, Mr. Ishida, for your explanation.

Ishida: Thank you.

Speaker: Yoshikazu Nunokawa (Corporate Director, Executive VP & GM)
Moderator: Koichi Yatsuda (VP, IR Department)

Yatsuda: Next, we would like to ask Mr. Nunokawa, who is the GM of the Global Business Platform Division and in charge of the Finance Division, to answer the questions regarding TEL's financial strategy. Thank you very much, Mr. Nunokawa. First, as the most frequently asked question regarding TEL's financial strategy, could you tell us your thoughts on the appropriate level of cash on hand and capital efficiency at TEL?

Nunokawa: First of all, we judge the level of our cash on hand not in absolute terms, but on an operational basis according to the business environment at the time, which is roughly two-and-a-half-to three months' worth. However, we believe that the level of cash on hand should be increased under the current situation where the business scale has been expanding for the past few years and there has been confusion in procurement.
As the semiconductor production equipment market expands, we believe that investment in R&D and other growth areas should be given top priority, and we aim to achieve a ROE target of 30% or higher in the medium-term management plan by increasing profits. We will continue to manage our balance sheet appropriately and aim to increase our corporate value.

Yatsuda: Thank you very much. You mentioned that TEL will prioritize investment in R&D and other growth areas, but R&D expenses have been increasing every year since FY2015. In FY2020, which was a period of market adjustment, TEL increased its R&D expenses despite a decline in net sales, and the ratio of SG&A expenses to net sales rose. How do you plan to control SG&A expenses in the future? Also, if you have an idea of the scale of R&D expenses in the future, please let us know.

Nunokawa: R&D expenses have increased beyond our plan, which was estimated to be 400 billion yen for the past three years. We will continue to invest in R&D at a high level in anticipation of the development of high value-added products. In addition to the current development projects related to our current business, we are also seeing an increase in corporate development projects for future growth. We categorize development targets into blocks, such as short-term development within three years, component research and development over five to ten years, and beyond, and manage the investment ratio of R&D expenses, including human resources. We will continue to invest in R&D, which is the source of our growth, without slowing down.

With regard to non-R&D expenses, we are accelerating our investment in internal core systems and DX with a view to improving productivity, and thereby increasing the efficiency of our operations.
In the area of DX, in addition to the existing Advanced Data Planning Department, which supports DX

activities for product competitiveness and customer response, the Digital Transformation Promotion Department was newly established in January this year to plan and support DX activities for productivity and management infrastructure.
By improving the efficiency of internal operations through company-wide deployment of new core systems and promotion of DX, we believe we can reduce the ratio of SG&A expenses to net sales and improve profitability in the future.

Yatsuda: Thank you very much. Lastly, could you tell us your current thoughts on the growth potential of profit margins in the next fiscal year and beyond, and the driving forces behind it?

Nunokawa: As I mentioned earlier, SG&A expenses, such as R&D expenses, have increased compared to our initial projection when we announced the medium-term management plan. This is due to the fact that the semiconductor production equipment market is growing faster than we had initially expected, and the speed of technological innovation is accelerating. We do not intend to achieve our target operating income margin by restraining investment in growth. Even if we temporarily improve our operating margin by restraining R&D expenses, it will not lead to a sustainable increase in corporate value. In the semiconductor production equipment market, which is expected to grow in the future, we would like to achieve the financial model targeted in the medium-term management plan by providing high value-added products and services, having our customers recognize the value of these products and services, and improving the profitability of each product and service.

Yatsuda: I now have a better understanding of TEL's approach to improving profit margins. Thank you very much for your time today, Mr. Nunokawa.

Nunokawa: Thank you.

Speaker: Tom Tsuneishi (Chairman of the Board)
Moderator: Koichi Yatsuda (VP, IR Department)

Yatsuda: Finally, Mr. Tsuneishi, Chairman of the board, would like to say a few words to everyone.

Tsuneishi: Thank you. My name is Tom Tsuneishi. Today, it was the first time for our IR team to host a Fireside Chat, and I hope it was a meaningful experience for everyone.

I am very grateful to all of you in the capital market for your daily support. And thank you very much for taking time out of your busy schedule to join us today.

We were awarded the 'Grand Prize Company' for Corporate Governance of the Year 2021, which is organized by the Japan Association of Corporate Directors. I would like to express my gratitude to all of you for your generous support. In addition, we were selected as one of the TOPIX Core 30 in October last year.

We have been recognized as a company that is growing globally in a rapidly expanding market. Thanks to your great support and cooperation, Tokyo Electron has grown to this level. However, the real work is yet to come, and I expect that we will continue to grow, and all of us in management will make our utmost efforts toward that end.

Though this is not global, but rather about the Tokyo Stock Exchange, we will be listed on the Prime Market this year, and we are considering various measures to comply with the revised Corporate Governance Code. Of course, the quality of management, strategies for growth, and their implementation are most important, but governance is also important for a company, and I believe that board governance, group governance, and all governance must be strong. To highlight our commitment to governance, it is now over 20 years since TEL established its Nomination Committee, Compensation Committee, and Ethics Committee.

All employees and management will make a concerted effort to achieve further growth toward the goal of becoming a world class company that is as globally competitive as possible, and I would like to ask for your continued support.

Thank you very much for your time today.